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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,602	02/27/2002	Yukiko Umemoto	XA-9634	7413

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EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n N . 10/083,602	Applicant(s) UMEMOTO ET AL.	
	Examiner Gene N Auduong	Art Unit 2818	

-- The MAILING DATE of this communication appears on th cover sheet with the c rrespondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Akaogi et al. (U.S. Pat. No. 5,761,127).

Regarding claim 6, Akaogi et al. disclose a flash-erasable semiconductor memory device comprising: (a) a memory cell comprising second semiconductor regions for a source and a drain, respectively, formed in a first semiconductor region in a semiconductor substrate (see figure 35, p-type second semiconductor region for memory device); a charge accumulation layer formed on a region between the second semiconductor regions for the source and the drain, through a gate insulating film (see figure 35); and a control electrode provided on the charge accumulation layer through an insulating film (figure 35, control electrode 122a provided on the charge accumulation layer 120a); (b) a third semiconductor region formed between the first semiconductor region and the semiconductor substrate (see figure 35, n-well region formed between the first and second regions); (c) first voltage application means for applying a voltage to the control electrode (figure 6, gate voltage generator); (d) a second voltage application

means for applying a voltage to the first semiconductor region (substrate voltage); and (e) a third voltage application means for applying a voltage to the third semiconductor region (figures 6, .drain/source voltage generator).

Regarding claims 7-10, Akaogi et al. disclose a flash-erasable semiconductor memory device comprising all of the limitation according to claim 6, wherein a first voltage is applied to the control electrode of the nonvolatile semiconductor memory (figure 6, gate voltage generator), and a second voltage is applied to the first semiconductor region (substrate bias generator, Vsub); and a potential difference between the first voltage and the second voltage corresponds to a voltage allowing electrons accumulated in the charge accumulation layer to be pulled out into the first semiconductor region (col. 7, lines 27+, col. 8, lines 42+, col. 24, lines 4+ and their related description).

Regarding claims 11-13, Akaogi et al. disclose a flash-erasable semiconductor memory device comprising all of the limitation according to claim 6, wherein the nonvolatile semiconductor memory comprises a plurality of memory cell groups each having a plurality of the memory cells formed therein, and the memory cells in each memory cell group are formed above a non-separated third semiconductor region (memory device having plurality of memory cell arrays, each array having plurality of cells, see figure 35).

Regarding claim 14, Akaogi et al. disclose a flash-erasable semiconductor memory device comprising all of the limitation according to claim 6, wherein the nonvolatile semiconductor memory further comprises means for determining a threshold voltage of the memory cell; a first voltage is applied to the control electrode and a second voltage is applied to the first semiconductor region during a first period, thereby allowing electrons accumulated in

the charge accumulation layer to be pulled out into the first semiconductor region; the threshold voltage of the memory cell is determined in a second period following the first period; if it is determined that the threshold voltage of the memory cell is higher than a predetermined threshold voltage, the first voltage is applied to the control electrode and the second voltage is applied to the first semiconductor region in a third period following the second period, thereby allowing the electrons accumulated in the charge accumulation layer to be pulled out into the first semiconductor region (col. 7, lines 27+, col. 8, lines 42+, col. 24, lines 4+ and their related description).

Regarding claim 15, Akaogi et al. disclose a flash-erasable semiconductor memory device comprising all of the limitation according to claim 14, wherein a third voltage is applied to the third semiconductor region during the first to third periods (col. 8, lines 10+).

Claims 20-29, 32-36, 1-5, 18-19 and 37-38 contains the similar limitation as previously discussed in claims 6-15. Therefore, they are analyzed as previously discussed with respect to claims 6-15.

Regarding claims 16-17, 30 and 31, the apparatus as previously discussed in claims 6-15, 20-29, 32-36, 1-5, 18-19 and 37-38 would be performed the method as claimed. Therefore, they are analyzed as previously discussed with respect to apparatus claims 6-15, 20-29, 32-36, 1-5, 18-19 and 37-38.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (703) 305-1343.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

GA
April 20, 2003

Gene N Auduong
Examiner
Art Unit 2818